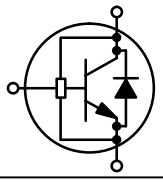
MJB18004D2T4

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

D2PAK For Surface Mount

POWER TRANSISTORS
5 AMPERES
1000 VOLTS
75 WATTS



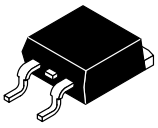
The MJB18004D2T4 is state–of–art High Speed High gain Bipolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window.

Main features:

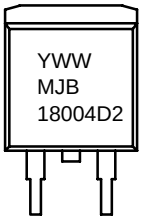
- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- “6 Sigma” Process Providing Tight and Reproductible Parameter Spreads

It’s characteristics make it also suitable for PFC application.

MARKING DIAGRAM



D²PAK
CASE 418B
STYLE 1



Y = Year
WW = Work Week

June, 2001 – Rev. 0
Publication Order Number:
MJB18004D2T4/D

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	1000	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter–Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5 10	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	°C/W
Junction to Ambient, When Mounted With the Minimun Recommended Pad Size.	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	450	547		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	1000	1100		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	12	14		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 500	μAdc
(V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 125°C				100	
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$		0.8 0.7	1 0.9	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.9 0.8	1 0.9	
Collector–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.38 0.55	0.5 0.75	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.45 0.75	0.75 1	
(I_C = 0.8 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C			0.9 1.6	1.5	
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C			0.25 0.28	0.5 0.6	
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	15 10	28 14		—
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		6 4	8 6		
(I_C = 1 Adc, V_{CE} = 2.5 Vdc)	@ T_C = 25°C @ T_C = 125°C		18 14	28 20		
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 Adc I_{B1} = 100 mA V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$	9 16	V
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		3.1 9	
	I_C = 2 Adc I_{B1} = 0.4 A V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C		11 18	
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		1.4 8	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS							
Forward Diode Voltage (I_{EC} = 1 Adc)		@ T_C = 25°C @ T_C = 125°C	V_{EC}		0.96 0.72	1.5	V
(I_{EC} = 2 Adc)		@ T_C = 25°C @ T_C = 125°C			1.15 0.8	1.7	
Forward Recovery Time (I_F = 0.4 Adc, di/dt = 10 A/μs)		@ T_C = 25°C	t_{fr}		440		ns
(I_F = 1 Adc, di/dt = 10 A/μs)		@ T_C = 25°C			335		
(I_F = 2 Adc, di/dt = 10 A/μs)		@ T_C = 25°C			335		
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)			C_{ob}		60	100	pF
Input Capacitance (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			C_{ib}		450	750	pF
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn–on Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 1 Adc V_{CC} = 250 Vdc	@ T_C = 25°C	t_{on}		500	750	ns
Turn–off Time		@ T_C = 25°C	t_{off}	1.1		1.4	μs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		100 150	150	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		1.15 1.6	1.3	μs
Turn–on Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		120 500	150	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}	1.85	 2.6	2.15	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{CC} = 15 V)							
Fall Time	I_C = 2.5 Adc I_{B1} = 500 mAdc I_{B2} = 500 mAdc V_Z = 350 V L_C = 300 μH	@ T_C = 25°C @ T_C = 125°C	t_f		130 300	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		2.12 2.6	2.4	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		355 750	500	ns
Fall Time	I_C = 2 Adc I_{B1} = 400 mAdc I_{B2} = 400 mAdc V_Z = 300 V L_C = 200 μH	@ T_C = 25°C @ T_C = 125°C	t_f		95 230	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	2.1	 2.9	2.4	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		300 700	450	ns
Fall Time	I_C = 1 Adc I_{B1} = 100 mAdc I_{B2} = 500 mAdc V_Z = 300 V L_C = 200 μH	@ T_C = 25°C @ T_C = 125°C	t_f		70 100	90	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		0.7 1.05	0.9	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		75 160	120	ns

TYPICAL STATIC CHARACTERISTICS

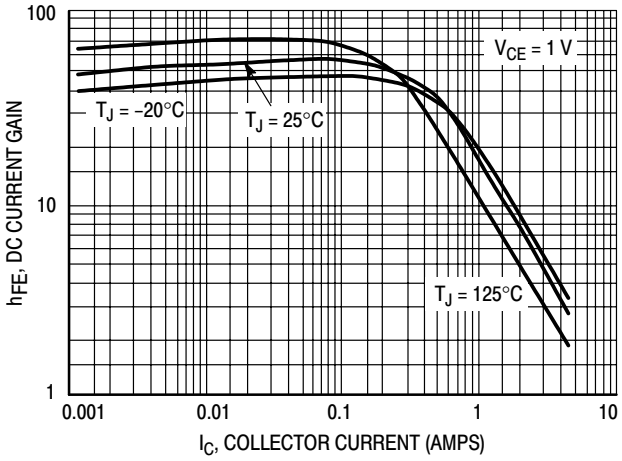


Figure 1. DC Current Gain @ 1 Volt

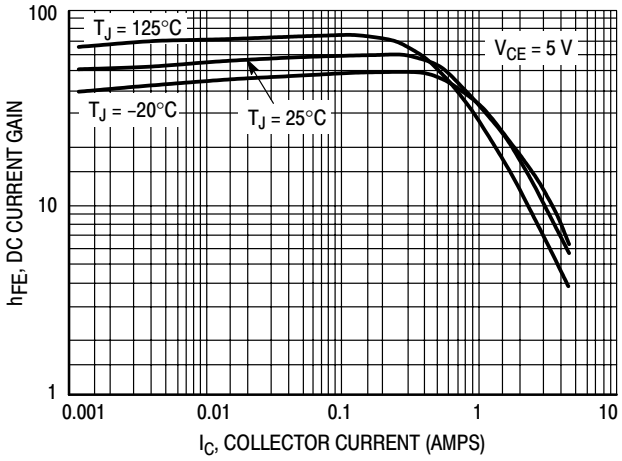


Figure 2. DC Current Gain @ 5 Volt

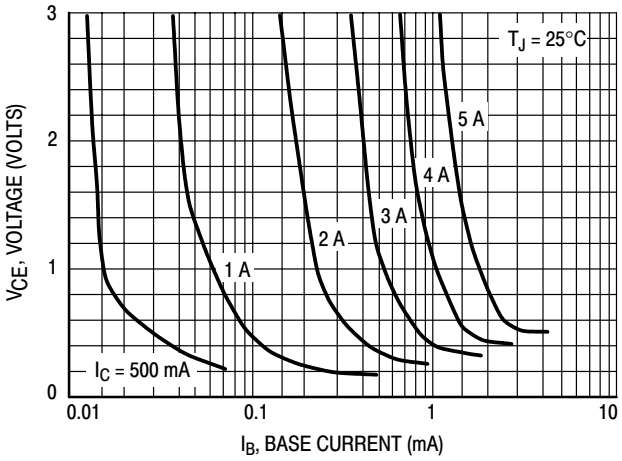


Figure 3. Collector Saturation Region

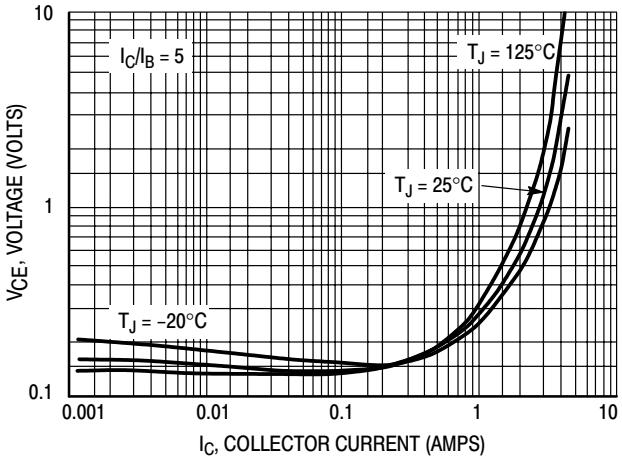


Figure 4. Collector–Emitter Saturation Voltage

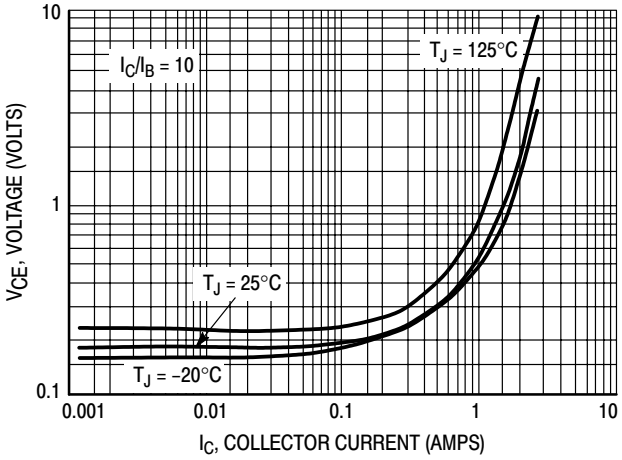


Figure 5. Collector–Emitter Saturation Voltage

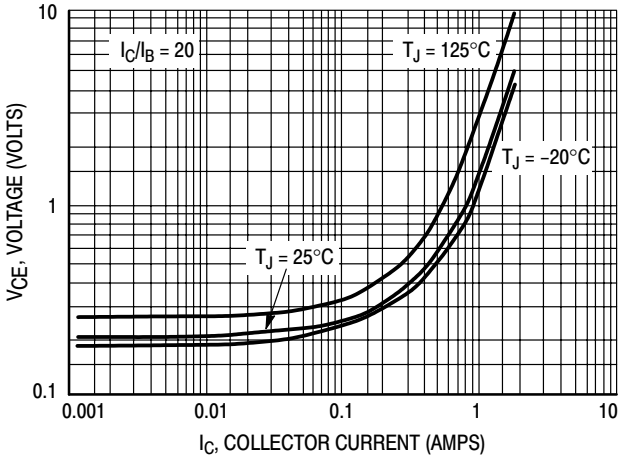


Figure 6. Collector–Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

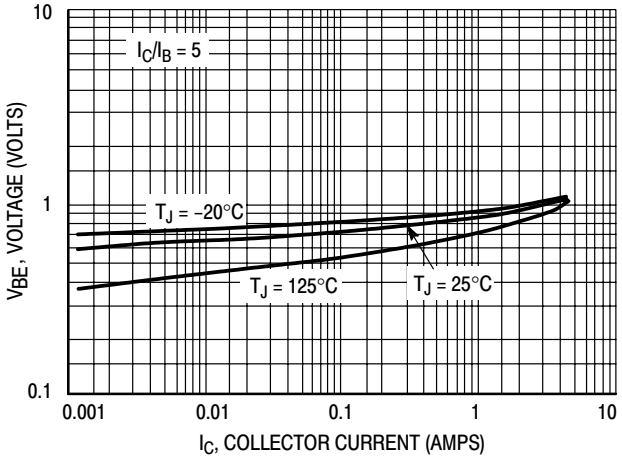


Figure 7. Base–Emitter Saturation Region

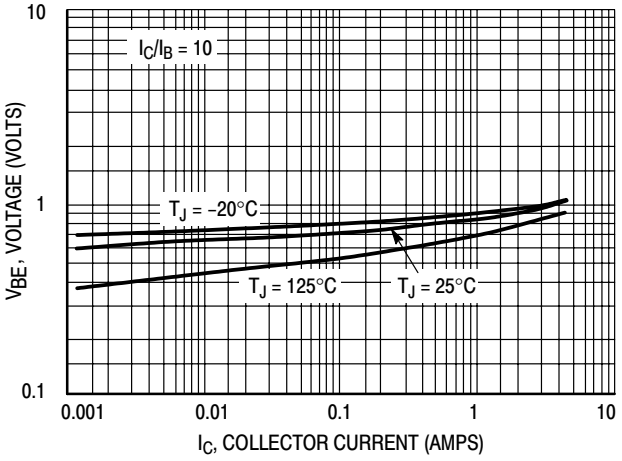


Figure 8. Base–Emitter Saturation Region

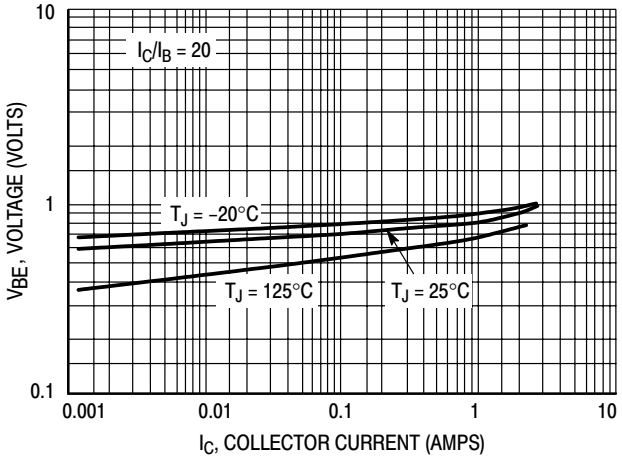


Figure 9. Base–Emitter Saturation Region

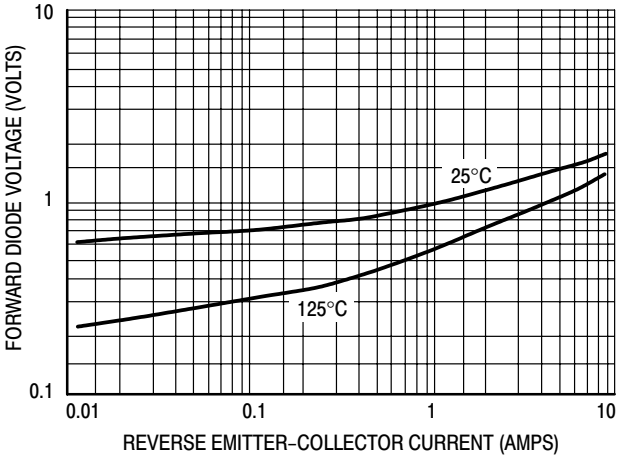


Figure 10. Forward Diode Voltage

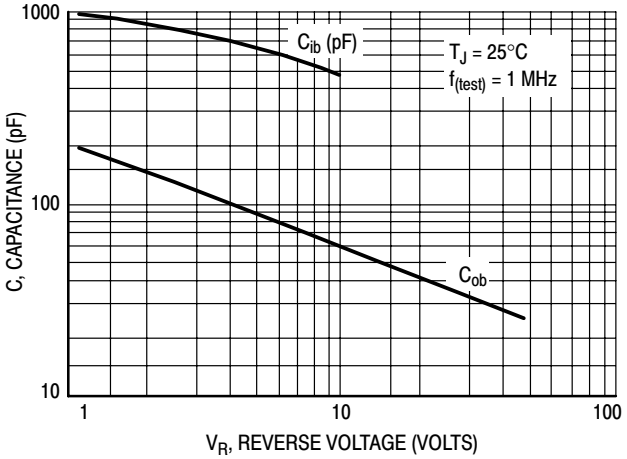


Figure 11. Capacitance

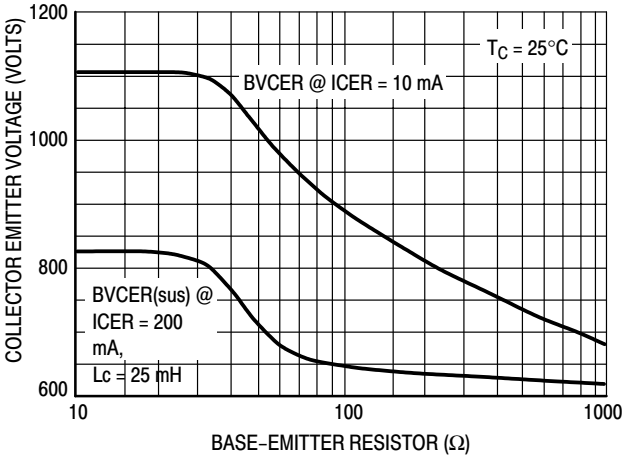


Figure 12. BVCER = f(R_{BE})

TYPICAL SWITCHING CHARACTERISTICS

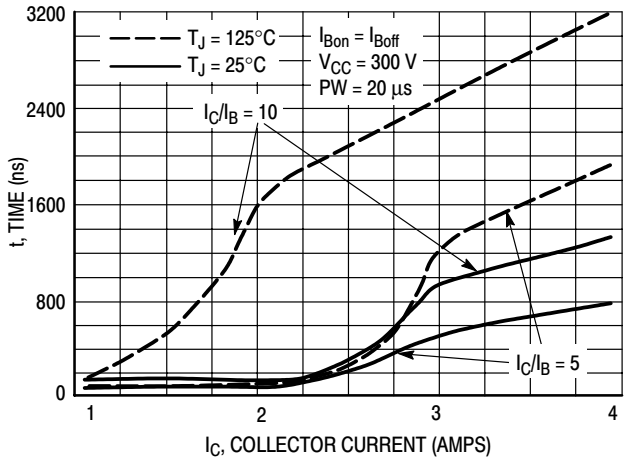


Figure 13. Resistive Switch Time, t_{on}

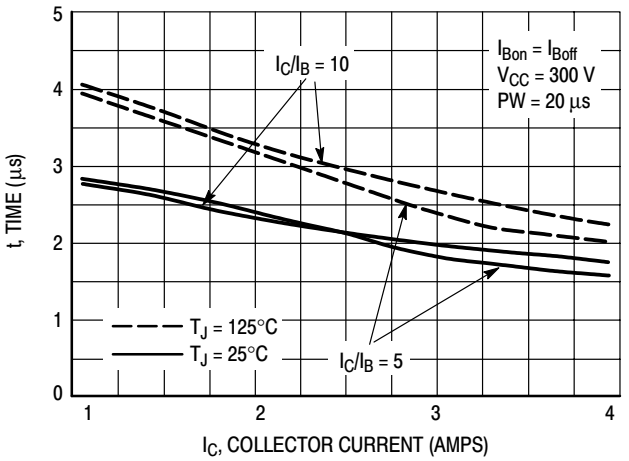


Figure 14. Resistive Switch Time, t_{off}

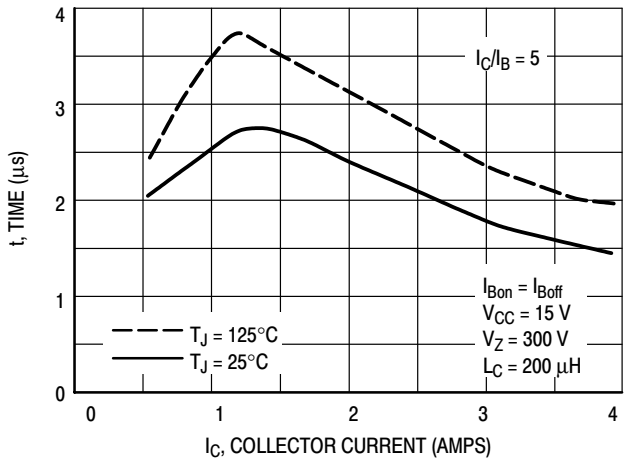


Figure 15. Inductive Storage Time, t_{si} @ I_C/I_B = 5

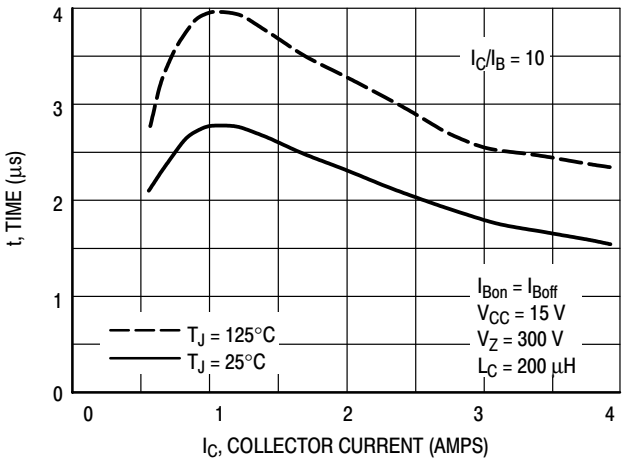


Figure 16. Inductive Storage Time, t_{si} @ I_C/I_B = 10

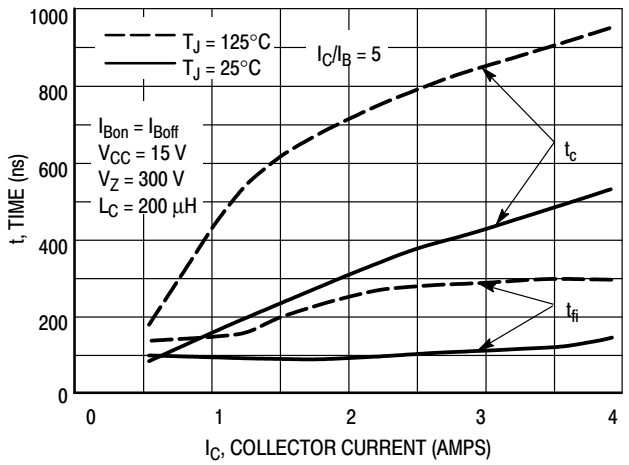


Figure 17. Inductive Switching Time, t_c and t_{fi} @ I_C/I_B = 5

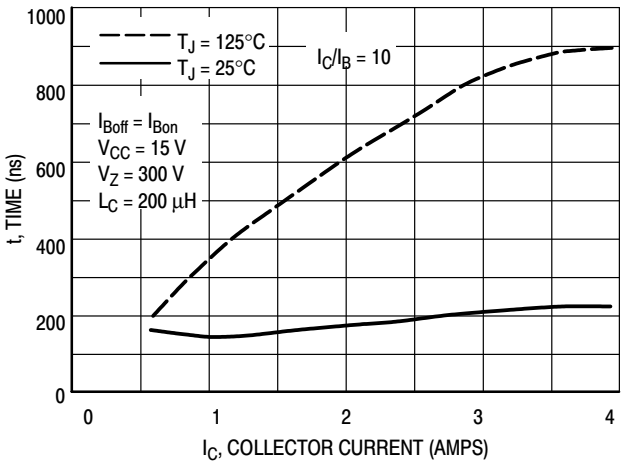


Figure 18. Inductive Switching Time, t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

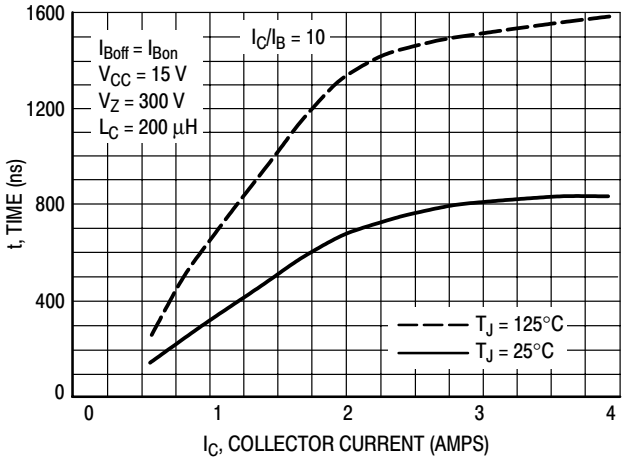


Figure 19. Inductive Switching, t_c @ I_C/I_B = 10

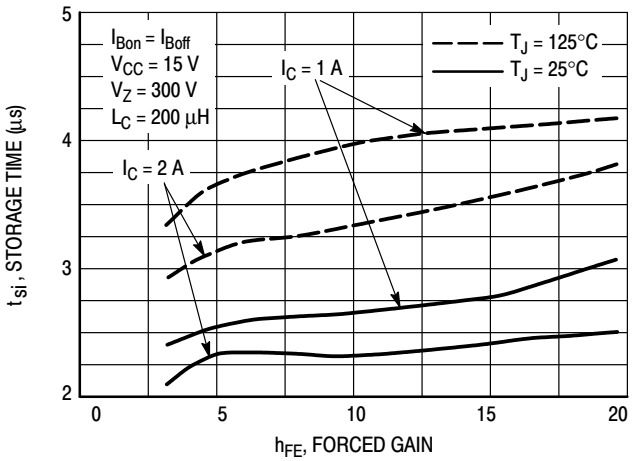


Figure 20. Inductive Storage Time

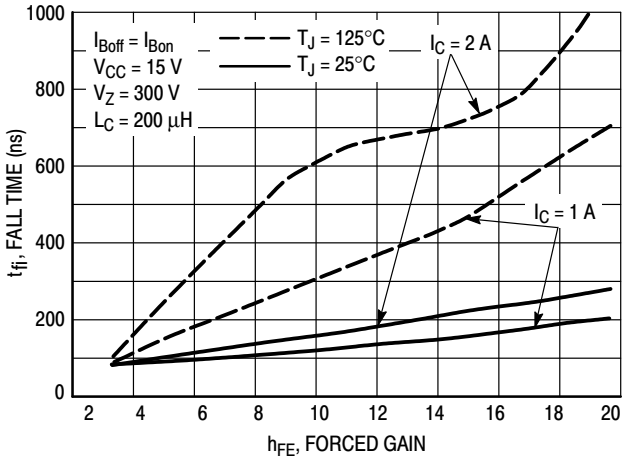


Figure 21. Inductive Fall Time

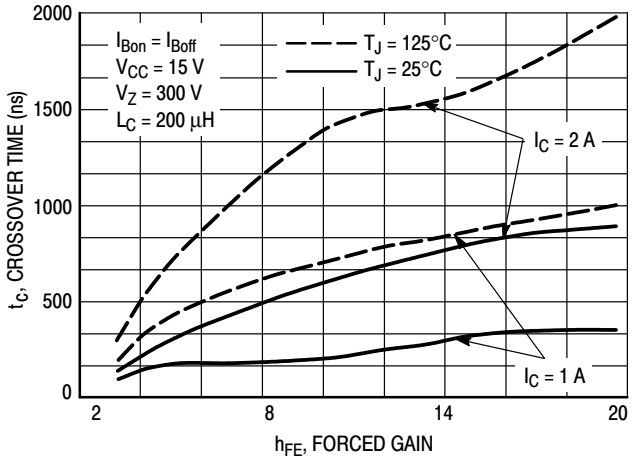


Figure 22. Inductive Crossover Time

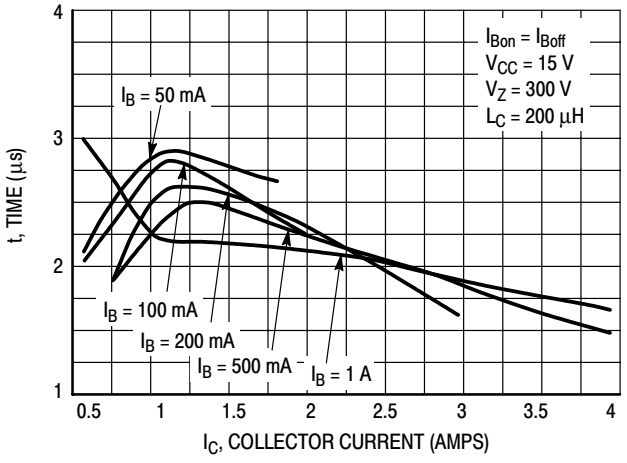


Figure 23. Inductive Storage Time, t_{si}

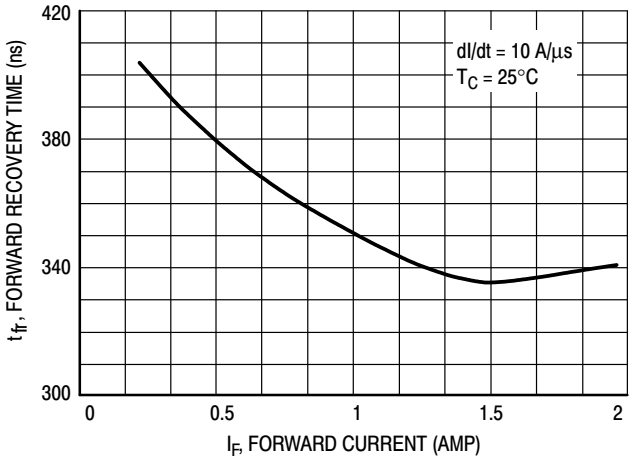


Figure 24. Forward Recovery Time, T_{FR}

TYPICAL SWITCHING CHARACTERISTICS

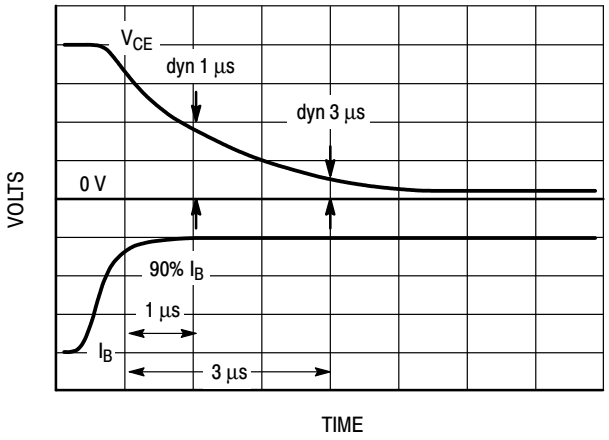


Figure 25. Dynamic Saturation Voltage Measurements

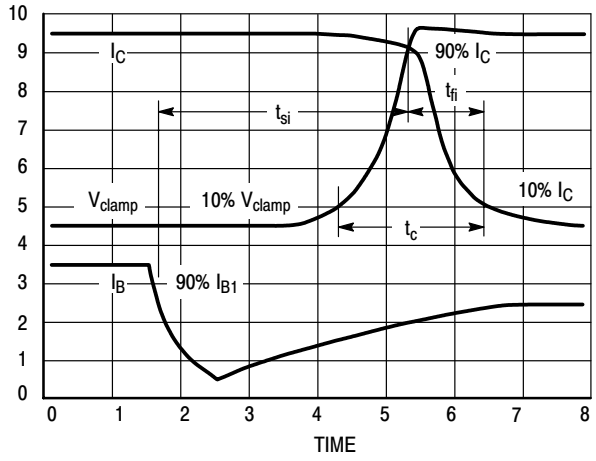


Figure 26. Inductive Switching Measurements

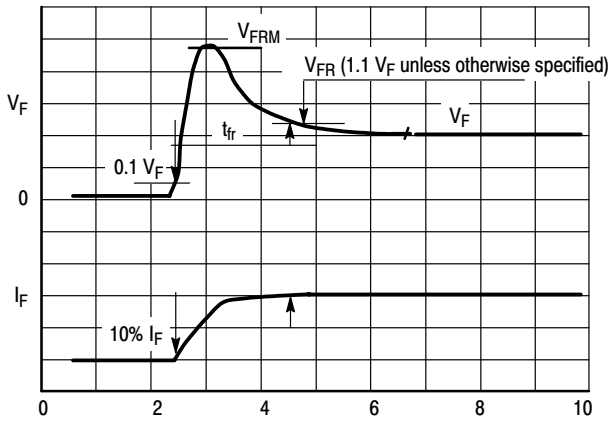
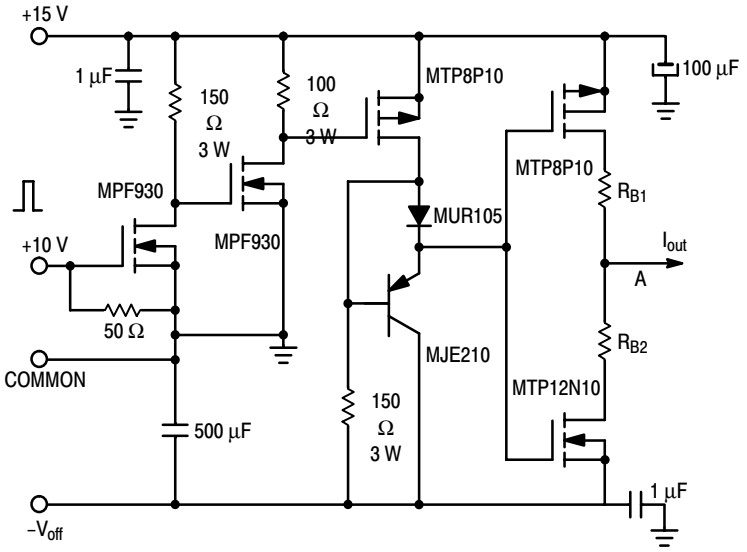
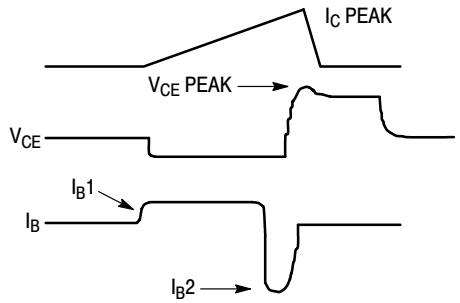


Figure 27. t_{fr} Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	RB1 selected for desired Ib1	RB1 selected for desired Ib1

TYPICAL CHARACTERISTICS

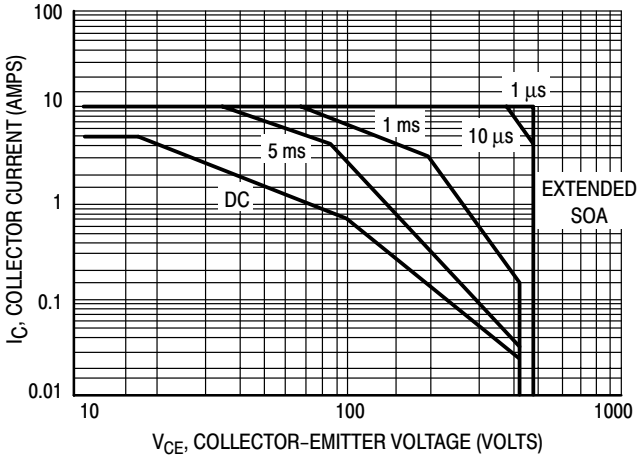


Figure 28. Forward Bias Safe Operating Area

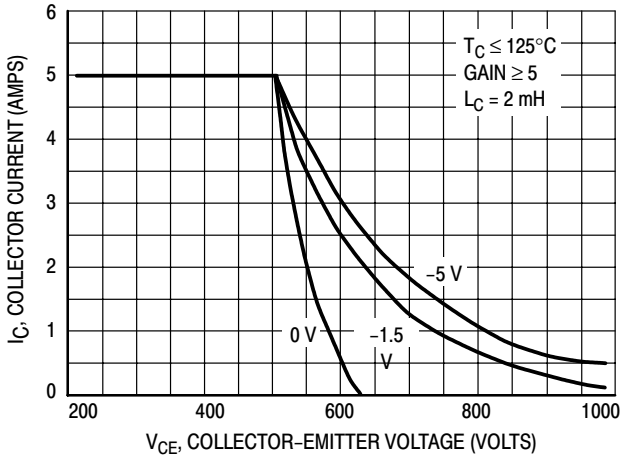


Figure 29. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

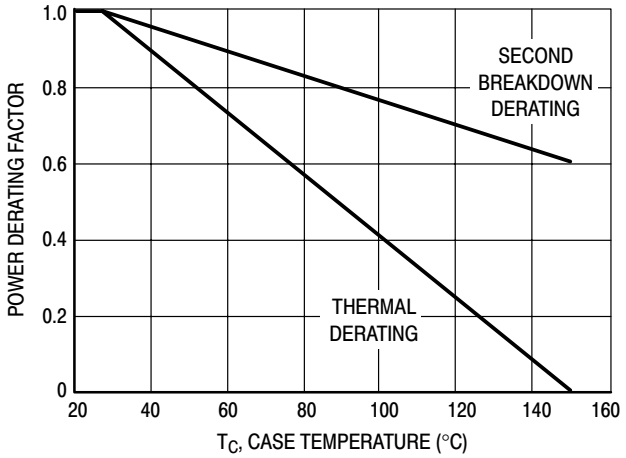


Figure 30. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

T_J(pk) may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse biased. The safe level is specified as a reverse–biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

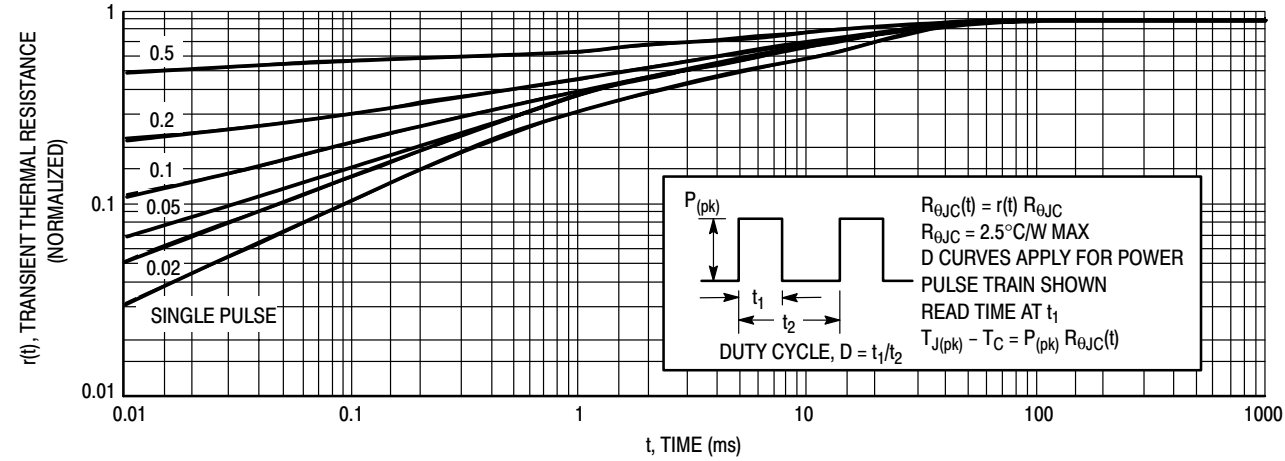
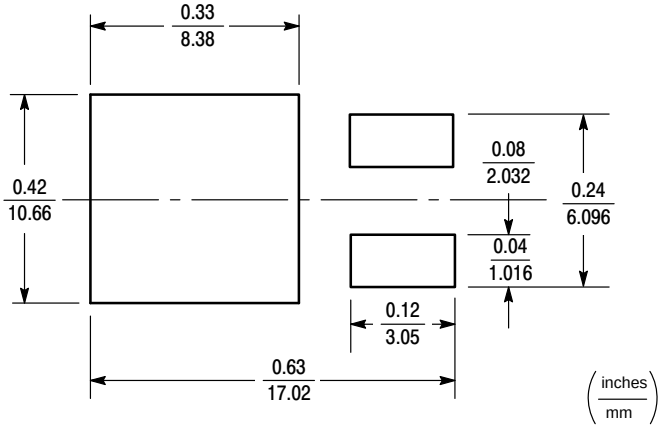


Figure 31. Typical Thermal Response ($Z_{\theta JC(t)}$) for MJB18004D2T4

INFORMATION FOR USING THE D²PAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the Collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For a D²PAK device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the D²PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the Collector pad. By increasing the area of the collection pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus Collector pad area is shown in Figure 32

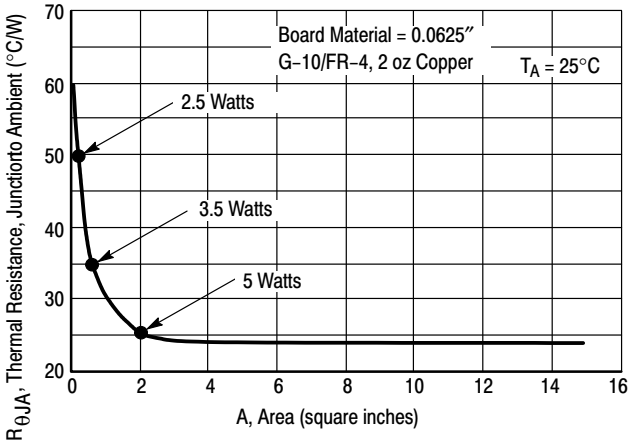


Figure 32. Thermal Resistance versus Collector Pad Area for the D²PAK Package (Typical)

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D^2PAK packages. If one uses a 1:1 opening to screen solder onto the Collector pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 33 shows a typical stencil for the DPAK and D^2PAK packages. The pattern of the opening in the stencil for the Collector pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

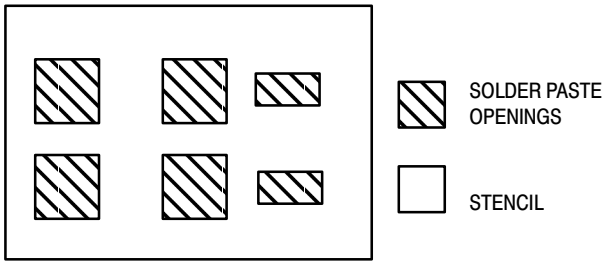


Figure 33. Typical Stencil for DPAK and D^2PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* * Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* * Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 34 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

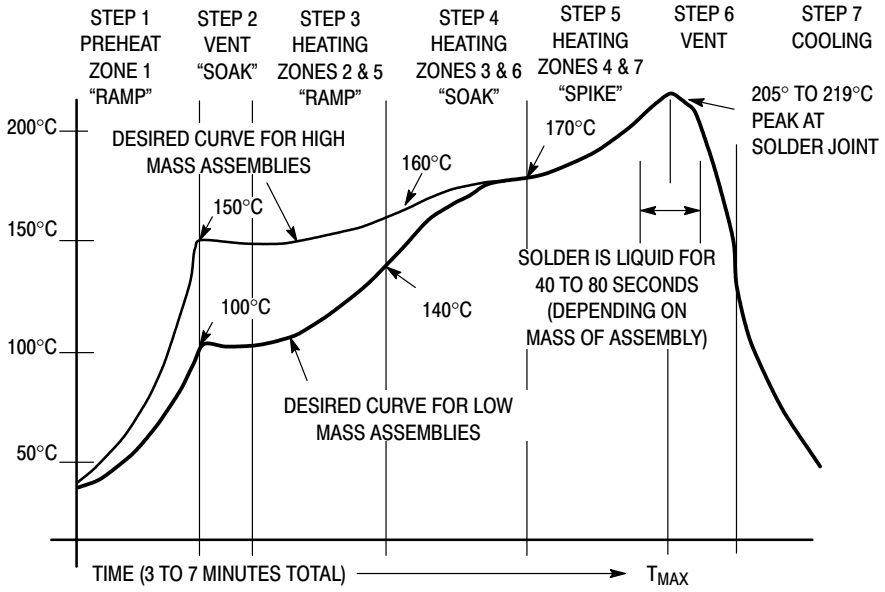
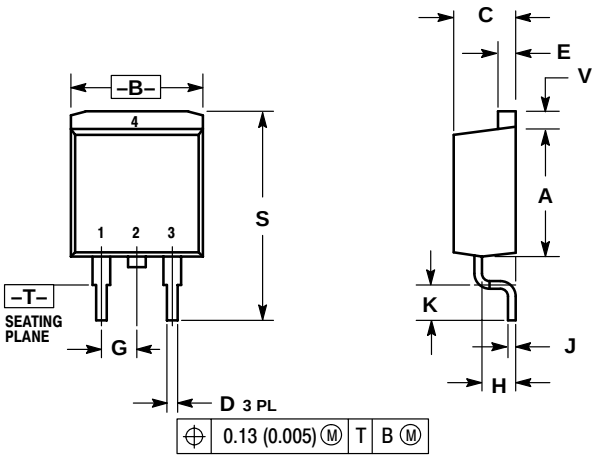


Figure 34. Typical Solder Heating Profile

PACKAGE DIMENSIONS

D²PAK
CASE 418B–03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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